ECEN 3730-
PCB Design,
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Lab 5 Report: SBB-build 555 timer

Introduction:

- In this lab, we will demonstrate the origin of switching noise in the power path and the role of loop inductance. By the end, we will deepen our understanding of switching noise in power delivery networks and how decoupling capacitors mitigate it.

Background:

- When IC's switch states, they create rapid changes in current ($\frac{dI}{dt}$) drawn from the power rail.
- This rapid current change interacts with the parasitic inductance of the power rail, causing switching noise (voltage noise) and a voltage droop.
- In this lab, we will measure and analyze these noise signals.

Circuit Overview (Slammer Circuit):

- A MCP601 MOSFET will act as a switch that creates a fast transient current
    - When the transistor is triggered, it "slams" the power rail by drawing a significant current
    - This transient current induces some voltage noise inside that power rail
- A resistor will limit the current and act as a place to measure the current in the circuit
- We will utilize two power rails; a 5V rail to power the Arduino and Op-Amp, and a 9V rail to power the slammer circuit by flowing current into the base of the transistor.
    - Arduino: Pin 13 will generate a PWM signal that will trigger the MOSFET.
        - The signal has a rise time of ~5ns.
- We use a IRF520 buffer to create a signal with a longer rise time (in the order of 1 μs) in order to draw a comparison.

Key Learning Objectives/Goals:

- Learn where switching noise comes from:
- Every voltage source can be modeled as a thevenin source:
    - Estimate thevenin source resistance of the VRM
    - Draw equivalent circuit model
- How decoupling capacitors reduce switching noise:
- Importance of rise time
- Important design considerations for a power delivery network (PDN):

BOM:

- Solderless breadboard
- 9V power supply
- Arduino (for 5V DC and PWM signal)
- MCP601 amplifier
- IRF520 MOSFET
- Short wires, 10 Ohm resistor
- Oscilloscope and scope probes

Step 1:

- We will use the arduino to generate a PWM signal with a 5% duty cycle (Ton = 1ms, Toff = 20ms) in order to limit the power dissipation.

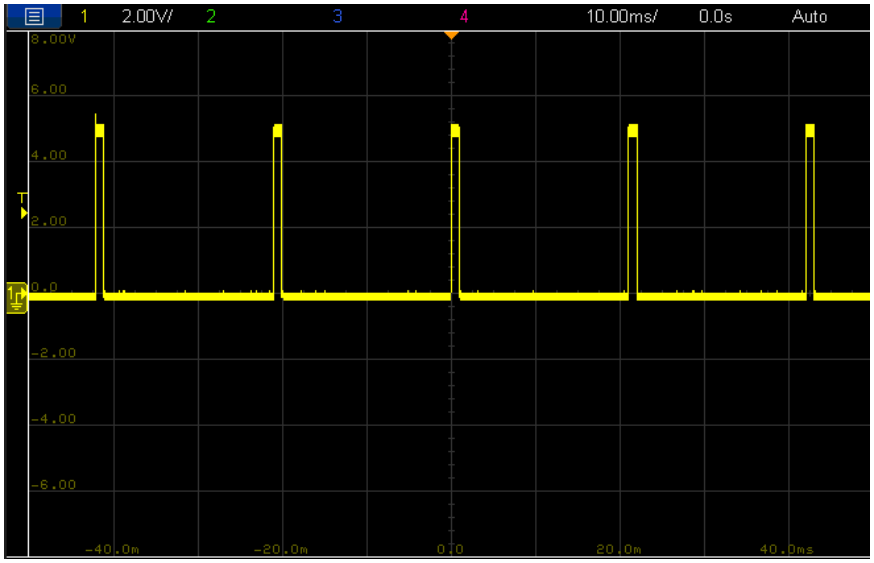

Figure 1: Shows the 5% Duty Cycle PWM Signal from PIN 13 of Arduino

Step 2:

- We build the slammer circuit, where when the transistor is triggered, current sinks through a 10-ohm resistor.
    - We will measure:
        - The two different inputs to the MOSFET–the direct PWM from the arduino (fast rise time), and the output coming from the Op-Amp buffer (slower rise time)
        - The current through the resistor
        - The voltage on the power rail (to observe the switching noise)

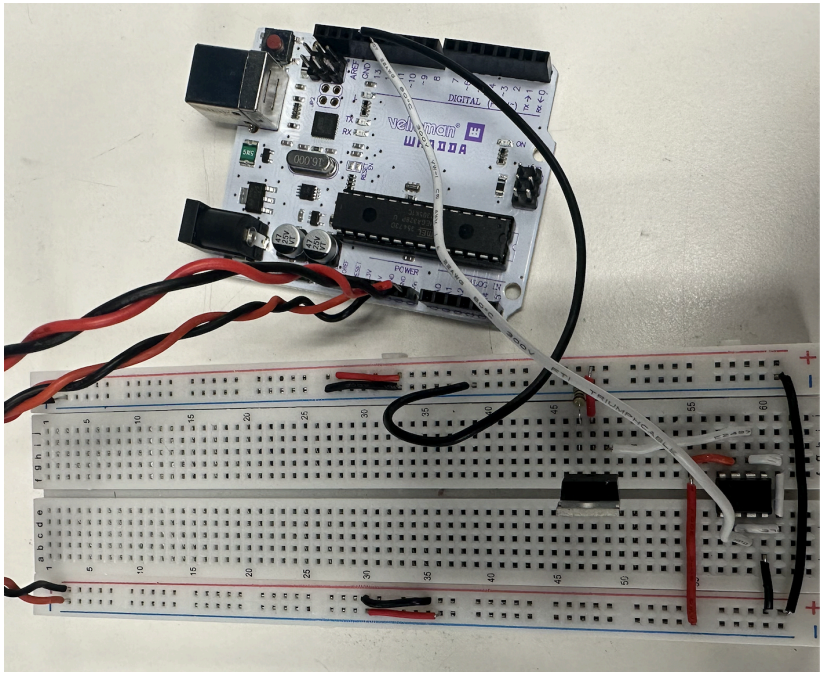

Figure 2: The completed slammer circuit on the SBB

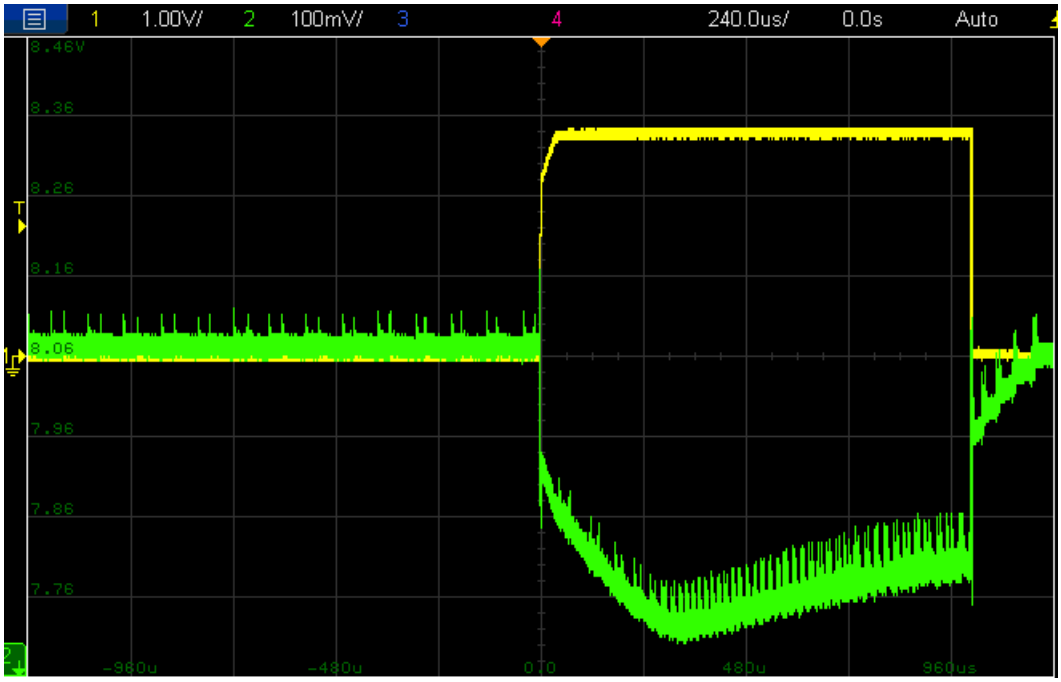

Figure 3: Shows the noise on the power rail (green line) & the voltage waveform on the source of the MOSFET (yellow line) coming from the Op-Amp

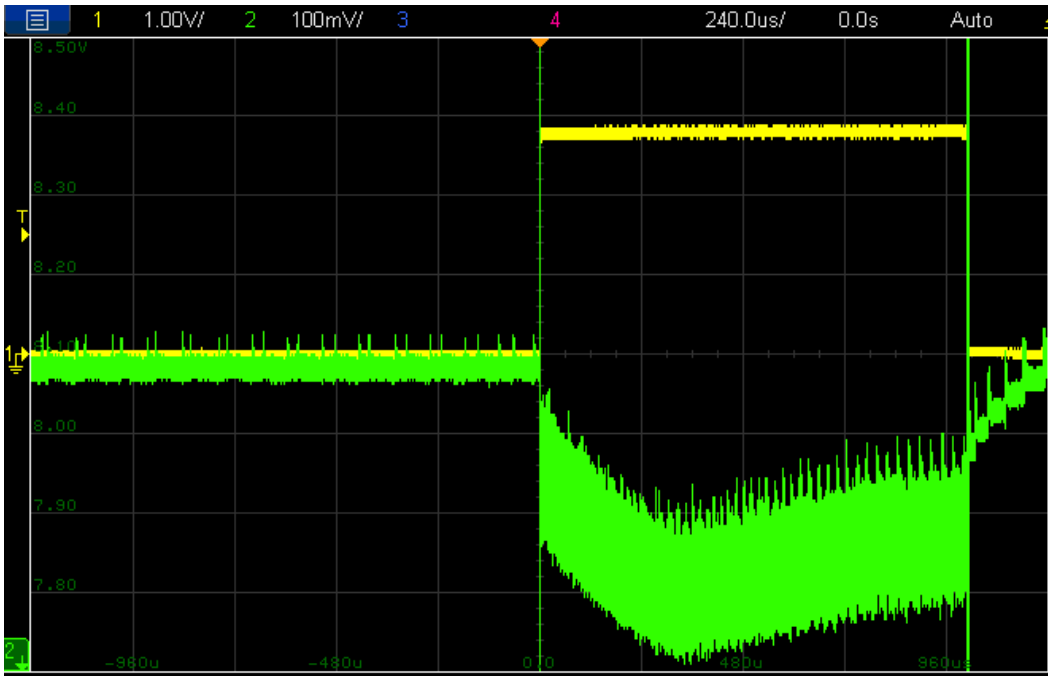

Figure 4: Shows the noise on the power rail (green line) & the voltage waveform on the source of the MOSFET (yellow line) coming directly from the PWM signal from PIN 13 on Arduino

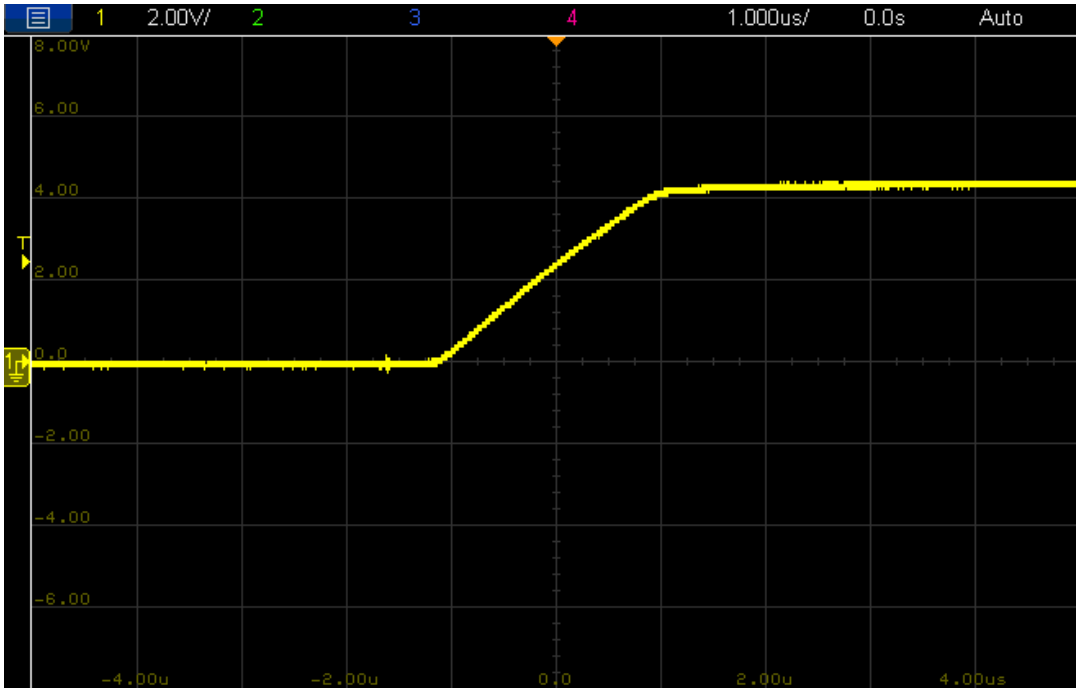

Figure 5: Shows the rise time of the Op-Amp output (~1µs, Slow)

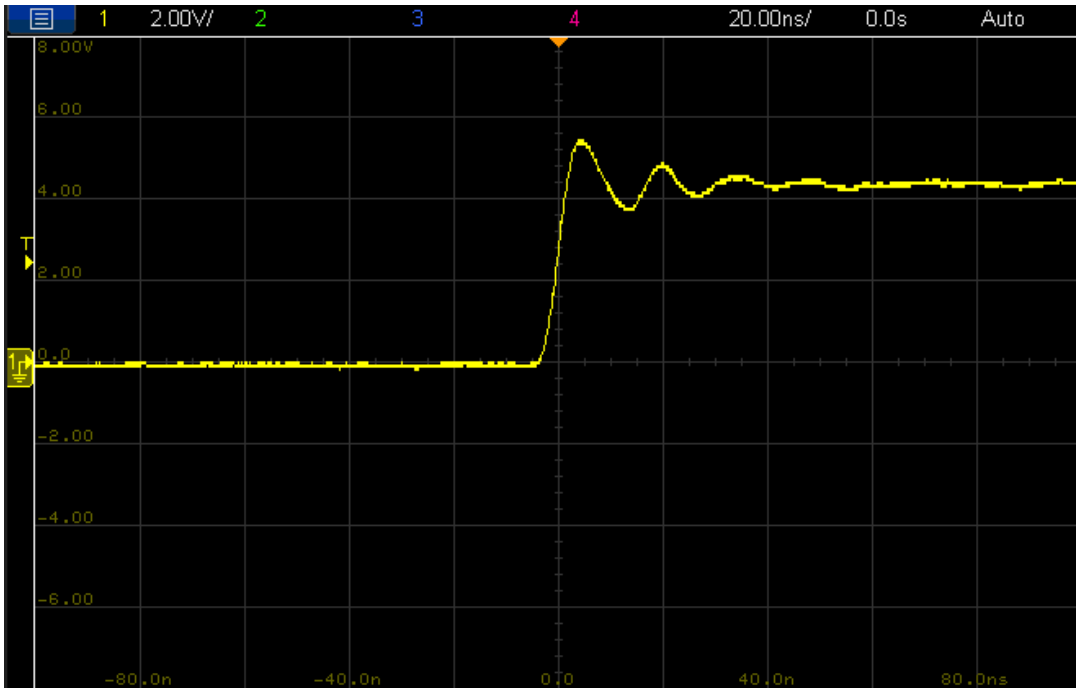

Figure 6: Shows the rise time of the Arduino output (~5ns, Fast)

When we compare the rise times and the switching noise between the two signals, we see that:

- Arduino Pin 13: Rise time ~5ns (Fast), so High ($\frac{dI}{dt}$), so a lot of switching noise (Figure 4)
- Output of Op-Amp: Rise time ~1µs (Slow), so Low ($\frac{dI}{dt}$), much less switching noise (Figure 3)

Step 3:

- Now we will measure the voltage across the resistor, find the current across it, and use those values to estimate the power dissipation in order to draw some important design conclusions.
- We will also find the voltage drop due to switching noise, and use this value to help find our thevenin equivalent
- We will also solve for the loop inductance
    - We will then draw an equivalent circuit model that includes both sources of impedance

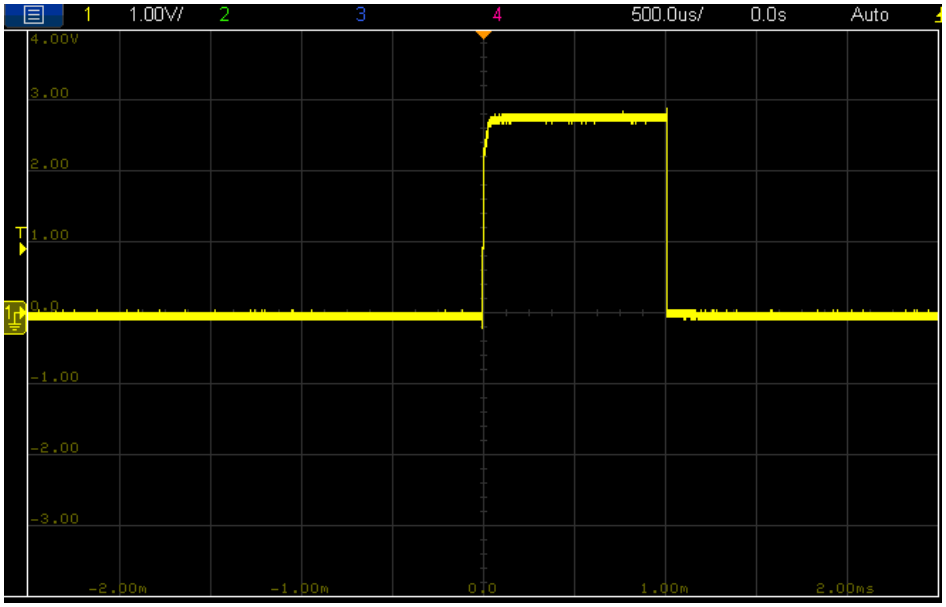

Figure 7: Shows the voltage waveform through the 10-Ohm resistor

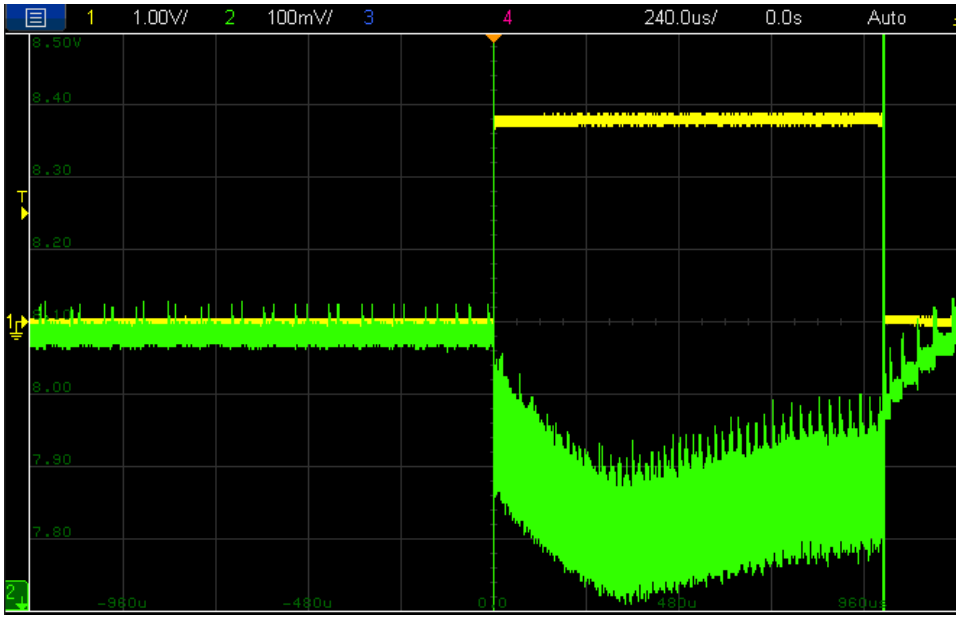

Figure 8: Shows the voltage drop in the noise. As seen, the green waveform (voltage on the drain pin/power rail) drops from ~8.1 V to ~7.7 V.

With roughly 2.9 V across the resistor, we can estimate the current through the resistor to be
$I = V/R \; -> \; I = 2.9/10 = 290\,mA$

$P = I^2R = (.290)^2(10) = \sim 0.85\,W$

I estimate that we see a power dissipation of roughly 0.85 W through our resistor. However, our resistor is only rated for 0.25 watts. This means that at DC, our resistor would blow very quickly. Hence, this stresses the importance of our 5% duty cycle PWM from the Arduino.

Thevenin Resistance: The voltage drop in the noise is (~0.4 V) and the current through the resistor is (~290mA). $Rth = Vth/I = 0.4\,V\,/0.29\,A = \sim 1.4\,\Omega$

However, our voltage drop is not only due to the resistance of the VRM. We also see impedance from parasitic inductance.

To break it down:

Voltage Droop (IR Drop) → Long-Term Drop

- This is the decrease in power rail voltage when the transistor turns on.
- It happens due to the Thevenin resistance in the VRM and power path.
- Relatively slow change and lasts as long as the transistor is conducting, then corrects.

Switching Noise (Voltage Spikes) → Short, Sharp Transients

- Short-lived spikes and dips that appear at the moment of switching.
- They happen due to parasitic inductance in the power rail, $\Delta V = L \cdot \frac{dI}{dt}$
- When the current changes very quickly (high $\frac{dI}{dt}$), inductance opposes this sudden change, creating sharp transient spikes.

If we see a voltage drop of ~8.1 V across the inductor, and the dI = 290mA, and the dt is ~5ns, then the loop inductance is $L = \Delta V/(\frac{dI}{dt}) = 8.1\,V\,/\,(\frac{0.29}{5ns}) = 140nH$

Why don't we see switching noise with the op-amp having a rise time of $\sim 1\mu s$?

The expected switching noise was $140nH \; * \; (0.29A/1\mu s) = 0.05\,V,$ too small a value to see compared to the pattern of the changing current.

Thus, our equivalent circuit model can be seen.

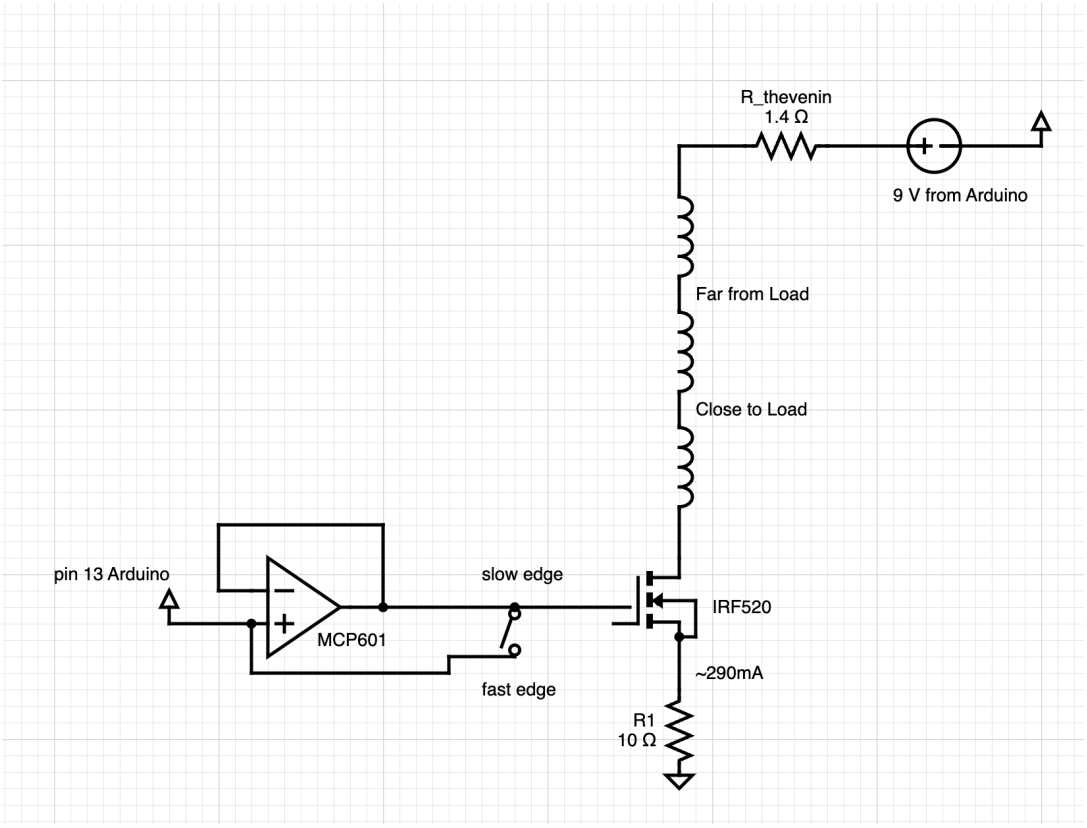

Figure 9: Shows equivalent model of circuit factoring in both sources of impedance, the parasitic inductance in the power rail & the thevenin resistance of the VRM.

Step 4:

Now, we will more closely observe the noise that is propagating in the power rail

- We will analyze the shape of the noise, seeing voltage droop & spikes due to the switching edges
- We will add decoupling capacitors of different values at different locations to see how well they help in mitigating the noise
- In each of the following measurements,
    - noise is measured on the drain pin to capture the switching edges
    - PWM voltage signal is measured on the source pin (sense resistor)

Figure 10: Shows yellow waveform (PWM signal on source pin), red waveform (Noise on power rail without a capacitor), and green waveform (noise on power rail with a 1µF capacitor placed far away)

Figure 11: Shows red waveform (1µF capacitor far from load) vs. green waveform (1µF capacitor close to the load)

-As seen, adding a *1µF* capacitor certainly mitigates some noise in the switching edges on the power rail.

-Now, we explore the effects of a 1000μF decoupling capacitor.

Figure 12: Shows red waveform (no decoupling capacitor) vs. green waveform(1000µF capacitor far away from the load)

Figure 13: Shows red waveform (1000µF capacitor far away from the load) vs. green waveform (1000µF capacitor close to the load)

As seen from the scope screenshots, a *1000μF* decoupling capacitor does a better job at mitigating the noise than a *1μF* decoupling capacitor. From both the *1000μF* and *1μF* experiments, it is clear that both the value and the location of the decoupling capacitor make an impact on their effectiveness. However, as we raise the value of our capacitor, our improvements become more and more negligible. We can conclude here that at a point (*> ~1000μF),* we no longer see a drastic improvement in the switching noise.

Now, we will inspect the voltage droop and overall noise both with and without a decoupling capacitor.

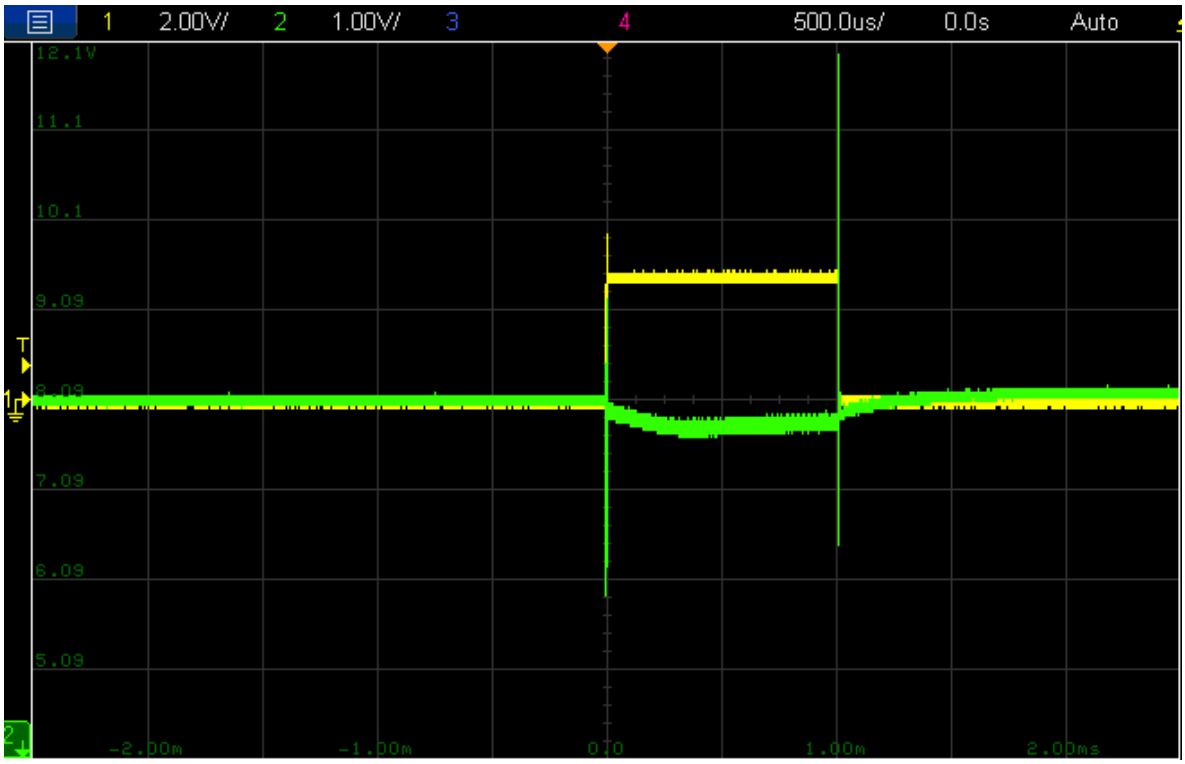

Figure 14: Zoomed-out scope screenshot showing the noise in the power rail (green waveform) and the transient switching spikes caused by parasitic inductance with NO capacitor present

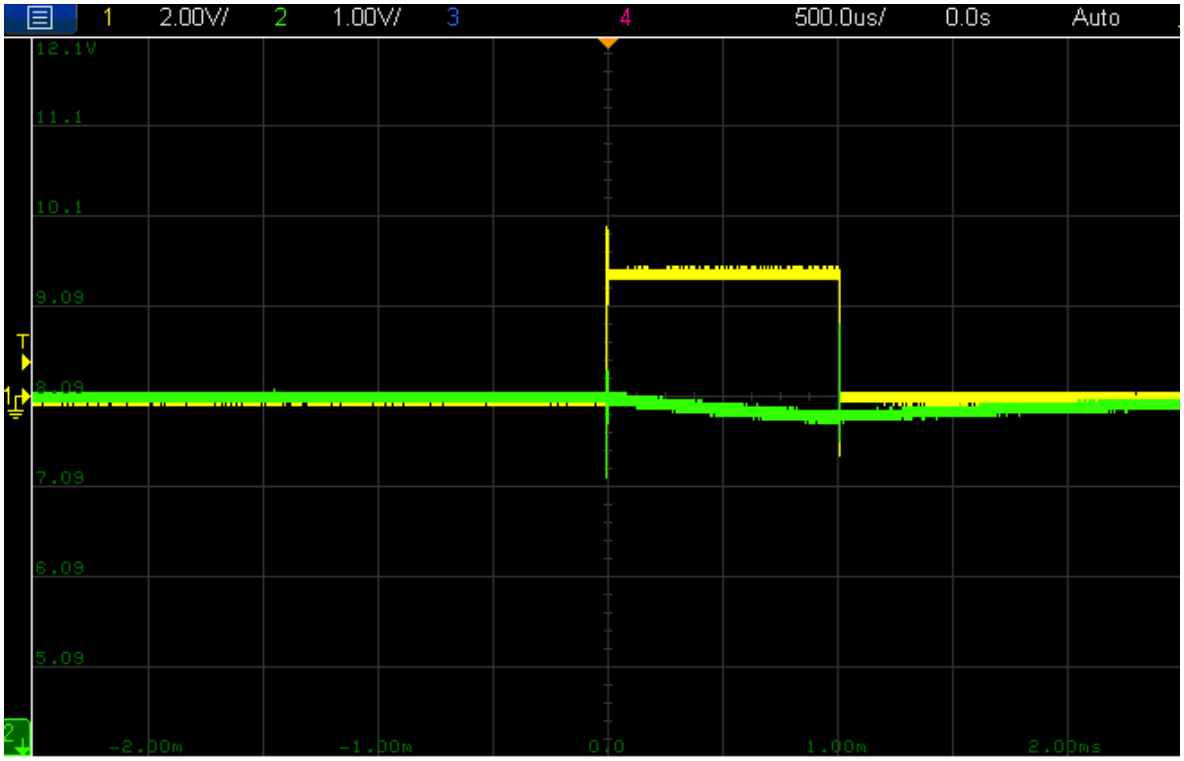

Figure 15: Zoomed-out scope screenshot showing the noise in the power rail (green waveform) and the transient switching spikes caused by parasitic inductance with a 1000µF decoupling capacitor present

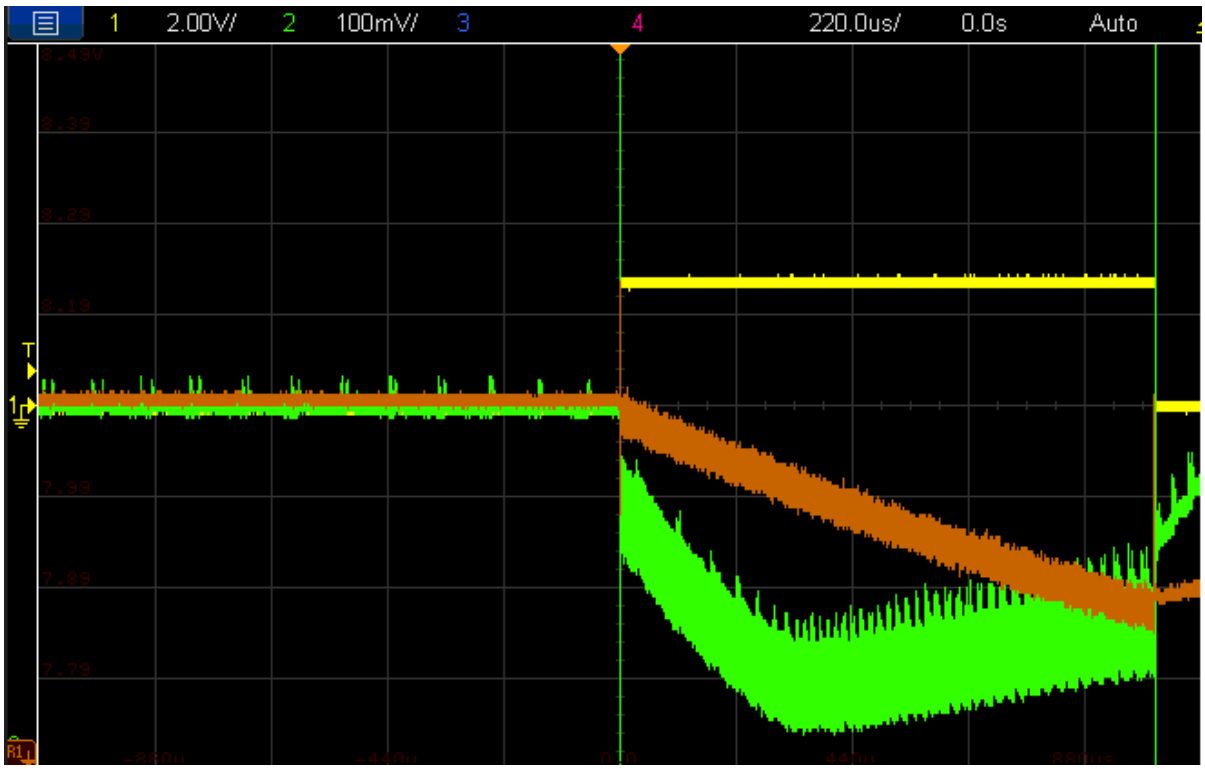

Figure 16: Scrope screenshot showing green waveform (noise without capacitor) and red waveform (noise with a 1000µF decoupling capacitor close to the load)

From these experiments, and as shown by the scope screenshots, we can conclude that a decoupling capacitor drastically reduces switching noise present in the power rail.

Conclusion/Learning Takeaways:

- This lab provided us valuable insights into switching noise, the stability of voltage within a power rail, transient currents, and important design considerations.
- Switching noise comes from transient current
    - Shorter rise time = more noise
        - In this case, the op-amp output provided a slow edge, resulting in a less severe transient, while the direct PWM signal showcased larger voltage noise and spikes due to a faster edge and higher $\frac{dI}{dt}$
            - This stresses the importance that the edge rate has on a circuit, especially in the presence of switching components
- I now understand the impact of parasitic elements on switching noise, such as the thevenin resistance of the VRM and the loop inductance of the power rail.
- Schematics/software often assume an ideal voltage source with ideal impedance, but it's important to consider real-world IR drops–voltage noise and spikes that must be accounted for.
- A decoupling capacitor reduces the noise by providing a local charge during the transient current.
    - A capacitor's effectiveness depends on its value and its placement
        - Capacitors closer to the IC/Load reduce noise more effectively because they do a better job of minimizing the loop inductance & providing charge faster
- Place the decoupling capacitors as close to the IC/load as possible
    - Use a good value for the expected ($\frac{dI}{dt}$)
    - Design PDNs with a low loop inductance and resistance
- Understanding the importance of rule #9 (making an educated prediction before measurement is taken) as well as the methods and tools to measure values on the oscilloscope are extremely important.
- The debugging process within this lab was also a key lesson. It's always important to take measurements at different locations to truly understand what's happening in the loop.
- Overall, this lab reinforced many fundamental concepts of PCB design, such as measurement techniques, power delivery, the ability to interpret oscilloscope data, and decoupling capacitors. Now that I feel comfortable with recognizing the impact of parasitic elements, I feel more confident in designing circuits–optimizing component placement, design trade-offs, and debugging strategies will be critical as we move forward in designing more robust boards.